Terms used **tracing disable interrupts buffer synchronization** Found **20,611** of **196,064**

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1 Characterizing the caching and synchronization performance of a multiprocessor operating system
Josep Torrellas, Anoop Gupta, John Hennessy
September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems ASPLOS-V**, Volume 27 Issue 9
Publisher: ACM Press
Full text available: pdf(1.52 MB) Additional Information: full citation, references, citings, index terms

2 The family of concurrent logic programming languages
Ehud Shapiro
September 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 3
Publisher: ACM Press
Full text available: pdf(9.62 MB) Additional Information: full citation, abstract, references, citings, index terms

Concurrent logic languages are high-level programming languages for parallel and distributed systems that offer a wide range of both known and novel concurrent programming techniques. Being logic programming languages, they preserve many advantages of the abstract logic programming model, including the logical reading of programs and computations, the convenience of representing data structures with logical terms and manipulating them using unification, and the amenability to metaprogrammin ...

3 A designer's perspective of the Hawk multiprocessor operating system kernel
V. P. Holmes, D. L. Harris
July 1989 **ACM SIGOPS Operating Systems Review**, Volume 23 Issue 3
Publisher: ACM Press
Full text available: pdf(1.60 MB) Additional Information: full citation, abstract, citings, index terms

The Hawk operating system kernel was specifically designed and implemented to support real-time applications on the SANDAC V embedded multiprocessor. The kernel provides a tasking model for program decomposition and supports message passing, synchronization, as well as other ancillary services. The kernel primitives have a Unix™-like system call interface to the C language and were designed to provide users a choice of level of abstraction, yet perform efficiently and behave predictabl ...

Terms used **trace buffer switching** Found **18,664** of **196,064**

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1 The effect of context switches on cache performance
Jeffrey C. Mogul, Anita Borg
April 1991 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , ACM SIGOPS Operating Systems Review , Proceedings of the fourth international conference on Architectural support for programming languages and operating systems ASPLOS-IV**, Volume 26 , 19 , 25 Issue 4 , 2 , Special Issue
Publisher: ACM Press
Full text available: pdf(1.08 MB) Additional Information: full citation, references, citings, index terms

2 Improving instruction supply efficiency in superscalar architectures using instruction trace buffers
Chih-Po Wen
April 1992 **Proceedings of the 1992 ACM/SIGAPP Symposium on Applied computing: technological challenges of the 1990's SAC '92**
Publisher: ACM Press
Full text available: pdf(898.33 KB) Additional Information: full citation, references, index terms

3 Design methodologies meet network applications: Analysis of power consumption on switch fabrics in network routers
Terry Tao Ye, Giovanni De Micheli, Luca Benini
June 2002 **Proceedings of the 39th conference on Design automation DAC '02**
Publisher: ACM Press
Full text available: pdf(565.86 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce a framework to estimate the power consumption on switch fabrics in network routers. We propose different modeling methodologies for node switches, internal buffers and interconnect wires inside switch fabric architectures. A simulation platform is also implemented to trace the dynamic power consumption with bit-level accuracy. Using this framework, four switch fabric architectures are analyzed under different traffic throughput and different numbers of ingress/egress ...

Keywords: interconnect networks, networks on chip, power consumption, systems on chip

Terms used **trace buffer switching synchronization** Found **25,287** of **196,064**

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1 Techniques for efficient inline tracing on a shared-memory multiprocessor
S. J. Eggers, David R. Keppel, Eric J. Koldinger, Henry M. Levy
April 1990 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1990 ACM SIGMETRICS conference on Measurement and modeling of computer systems SIGMETRICS '90**, Volume 18 Issue 1
Publisher: ACM Press
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

While much current research concerns multiprocessor design, few traces of parallel programs are available for analyzing the effect of design trade-offs. Existing trace collection methods have serious drawbacks: trap-driven methods often slow down program execution by more than 1000 times, significantly perturbing program behavior; microcode modification is faster, but the technique is neither general nor portable. This paper describes a new tool, called MPTRACE, for collecting tr ...

2 Improving AP1000 parallel computer performance with message communication
Takeshi Horie, Kenichi Hayashi, Toshiyuki Shimizu, Hiroaki Ishihata
May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture ISCA '93**, Volume 21 Issue 2
Publisher: ACM Press
Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, references, citings, index terms

The performance of message-passing applications depends on cpu speed, communication throughput and latency, and message handling overhead. In this paper we investigate the effect of varying these parameters and applying techniques to reduce message handling overhead on the execution efficiency of ten different applications. Using a message level simulator set up for the architecture of the AP1000, we showed that improving communication performance, especially message handling, improves tota ...

3 Modeling issues in the design of embedded systems: An IDF-based trace transformation method for communication refinement
Andy D. Pimentel, Cagkan Erbas
June 2003 **Proceedings of the 40th conference on Design automation DAC '03**
Publisher: ACM Press
Full text available: pdf(186.11 KB) Additional Information: full citation, abstract, references, citings, index